IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A processor embedded with other circuitry as part of an application specific integrated circuit, the processor comprising:

- a control ~~control means for controlling~~ circuit operable to control operations within the processor in accordance with a stored program, the program comprising stored instructions selected from a predetermined instruction set;
- a plurality of registers for storing calculated values;
- an addressing ~~means~~ circuit operable under control of the stored instructions to perform addressing operations addressing a data storage space of the processor, at least one said registers being operable as an address register as part of the addressing ~~means~~ circuit for storing calculated address values for use in said addressing operations;
- a common arithmetic unit having input and output data paths each of width n bits, and being operable under control of the stored instructions both to calculate general data values in co-operation with the registers, and to calculate address values in co-operation with said address register;

wherein

- at least one of said registers is operable as a wide data register of width substantially greater than n bits for storing results of arithmetic operations wider than n bits; and
- a shifting circuit of said greater width is interposed between the output path of the arithmetic unit and the wide data register, with a feedback path also of said greater width from data outputs of the wide data register, and is operable under control of the stored instructions to generate a shifted result of said greater width in the wide data register in response to at least a multiplication, division or normalisation instruction, by repeated operation of the arithmetic unit in cooperation with the shifting circuit and the wide data register.

2. (Original) A processor according to claim 1, wherein said wide data register comprises a pair of data registers (AH,AL) each of width n, independently connectable to an input or output path of said arithmetic unit.

3. (Currently Amended) A processor according to claim 1, wherein said control ~~means~~ circuit is responsive to a predetermined multiplication instruction to control the arithmetic unit, the shifting circuit and the wide data register so as to multiply two values of width n bits, the result being obtained in the wide data register after plural operating cycles of the arithmetic unit and the shifting circuit, the number of cycles being independent of the actual values being multiplied.

4. (Currently Amended) A processor according to claim 1, wherein said control ~~means~~ circuit is responsive to a predetermined division instruction to control the arithmetic unit, the shifting circuit and the register so as to divide two values of width n bits, the quotient and remainder being obtained in the wide data register after plural operating cycles of the arithmetic unit and the shifting circuit, the number of cycles being independent of the actual values being divided.

5. (Original) A processor according to claim 1, wherein the shifting circuit can perform only single bit position shifting per operating cycle.

6. (Original) A processor according to claim 1, formed in an integrated circuit together with program storage and data storage space addressable independently via respective address buses of the processor, wherein the processor is arranged to execute instructions that have been selected from the instruction set and stored in the program storage space of the integrated circuit.

7. (Currently Amended) A processor according to claim 1, wherein the ~~instruction~~ instructions of the instruction set are of fixed length.

8. (Original) A processor according to claim 1, wherein the execution of each instruction takes a number of processor execution cycles, dependent on the type of instruction, and wherein a further instruction is not executable until such instructions are completely executed.

9. (Original) A processor according to claim 1, wherein, to the extent that it can be provided under program control, data communication externally of the processor is possible only via the data storage address space.

10. (Original) A processor according to claim 1, wherein an instruction to store data from one of said data registers to said data storage space is executed using a data path not including the arithmetic unit.

11. (Original) A processor according to claim 1, wherein dedicated unidirectional data paths are provided (i) between the register outputs and an input path of the arithmetic unit and (ii) between the arithmetic unit output data path and the register input.

12. (Original) A processor according to claim 11, wherein a further dedicated path is provided to one address register (X) of the processor from a program counter register (PC), said data path including an incrementer, so as to store a subroutine return address.

13. (Original) A processor according to claim 1, without an interrupt routine execution handling facility.

14. (Original) A processor according to claim 1, further comprising an interface for receiving a communication request from external circuitry, the processor being responsive to such a communication request only during predetermined time periods during normal program controlled operation.

15. (Original) A processor according to claim 14, wherein said predetermined periods are defined by inclusion of a predetermined communication instruction in the stored program.

16. (Original) A processor according to claim 1, wherein the processor has at least one external control line, and wherein at least one instruction of the instruction set is decoded differently depending on a signal present on the external control line.

17. (Currently Amended) A processor according to claim 1, wherein the processor has a basic instruction cycle sub-divided into plural internal clock states, and wherein, for at least one combinational logic circuit having plural input lines and functioning under control of each stored program, ~~means~~ sample and latch circuits are provided to sample and latch input values for the combinational logic circuit only at a defined state or states within the instruction cycle.

18. (Original) A processor according to claim 17, wherein said combinational logic circuit comprises the arithmetic unit of the processor.

19. (Currently Amended) A processor according to claim 18, wherein said combinational logic circuit further comprises an instruction decoding circuit of the control ~~means~~ circuit.

20. (Original) A processor according to claim 1, wherein n is sixteen.

21. (Currently Amended) A processor according to claim 1, adapted to operate under control of a program including a pre-stored linear sequence of instructions and a high frequency clock signal, the processor further comprising ~~means for implementing~~ a power control circuit operable to implement a state of low power consumption in which execution of said program is suspended, and ~~means for ending~~ operable to end said suspended state so that execution of said program continues from the next instruction in the stored sequence without execution of instructions stored outside said sequence.

22. (Original) A processor according to claim 21, wherein said suspended state is entered in accordance with a signal (WAKE_UP) applied to the processor, but only at a point in the instruction sequence defined by inclusion of a specific instruction.

23. (Currently Amended) A processor according to claim 1, adapted to operate synchronously under control of a high frequency clock signal, the processor further comprising:

- ~~means for imposing~~ a power control circuit operable to impose a state of low power consumption in which execution of said program is suspended and said clock signal is isolated from the processor circuitry, while the clock signal continues running; and
- ~~monitoring means~~ a monitor responsive to any of a plurality of external signals ~~for ending~~ and operable to end said suspended state by re-applying said clock signal to the processor,

wherein said ~~monitoring means~~ monitor comprises:

- plural individual monitoring circuits for detecting predetermined changes in respective ones of the external signals; and
- a common trigger circuit responsive to outputs of the individual monitoring circuits ~~for re-applying~~ and operable to re-apply said clock signal to the processor,

and wherein the individual monitoring circuits, but not the common trigger circuit, are isolated from the running clock signal during said suspended state.

24. (Currently Amended) A processor according to claim 23, wherein at least one of said individual monitoring circuits comprises:

- ~~means~~ a storage circuit responsive to said clock signal prior to the suspended state ~~for storing~~ and operable to store a value of the corresponding external signal; and
- an asynchronous circuit ~~means for~~ operable, during the suspended state, ~~comparing~~ to compare the external signal with the ~~stored~~ value stored by said storage circuit.

25. (Currently Amended) A processor according to claim 1, wherein the integrated circuit has at least one external control line (RUN_STEP), and wherein at least one instruction (BRK) of the instruction set is an instruction which will either halt the program-controlled processing operations or will effect no meaningful operation, depending on ~~said signal~~ a signal on said external control line.

26. (Currently Amended) A processor according to claim 25, comprising ~~means~~ an output (RUN_STEP) ~~for signalling~~ operable to signal externally that execution has been halted.